

Notice of Allowability

Application No.

10/662,025

Examiner

Venkatesh Haliyur

Applicant(s)

CHAPMAN, JOHN T.

Art Unit

2619

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendments of 12/03/2007.
2. ☒ The allowed claim(s) is/are 1-6, 9-12, 15, 16 and 19-22.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of the:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____ |

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should ~the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.
2. Authorization for this examiner's amendment was given in a telephone interview with Stephen S Ford (Reg No: 35,139) on 02/14/2008.
3. The application has been amended as follows:

In claims:

a) Claims 1, 10, 11, 15, 16, 19, 20 have been amended to recite as follows:

1. A synchronization circuit, comprising:
 - a local timestamp counter configured to generate a local timestamp value;
 - a processing circuit to receive externally generated synchronization pulses and to receive a predicted master time stamp value associated with a future one of the externally generated synchronization pulses, wherein the processing circuit

receives the predicted master timestamp value asynchronously in Internet Protocol (IP) packets received over an IP connection,

the processing circuit to identify the local timestamp value and synchronize the local timestamp value upon receipt of the future one of the externally generated synchronization pulses; and

one or more line cards in a same Cable Modem Termination System (CMTS) chassis that each have local timestamp counters that is adjusted according to the received predicted master timestamp value and local timestamp value at the future received synchronization pulse and wherein the processing circuit identifies an error condition according to a number of times the local timestamp counter is synchronized with the received predicted master timestamp value.

10. A synchronization system, comprising:

a first Cable Modem Termination Systems (CMTS) having a first chassis containing a master synchronization circuit;

a second CMTS having a second separate chassis containing a slave synchronization circuit;

a master synchronization circuit including:

a master counter to generate respective master timestamp values varying with cycling of a clocking signal;

a processing circuit to determine, for a given count of consecutive ones of synchronization pulses cycling less often than the clocking signal, the corresponding difference between the master timestamp values and to

calculate a future master timestamp value by adding the corresponding difference to an initial one of the master timestamp values corresponding to an initial one of the synchronizing pulses and the master synchronization circuit being configured to

forward the calculated future master timestamp value to the slave synchronization circuit over a wide area network for synchronizing the value of a slave counter in the slave synchronization circuit with the future master timestamp value at a future synchronization pulse generated independently of operations by the master counter and slave counter and corresponding to a given count of consecutive ones of synchronization pulses following the initial one of the synchronization pulses; and

one or more line cards in at least one of the first and second CMTS that include one or more slave circuits each synchronized with the future master timestamp value at the future synchronization pulse when the difference between an actual master timestamp value and the future master timestamp value is within the predetermined range.

11. The system according to claim 10 wherein the master synchronization circuit is further configured to:

identify the actual master timestamp value corresponding to the future synchronization pulse when the future synchronization pulse occurs;

determine whether a difference between the actual master timestamp value and the future master timestamp value is within a predetermined range;
and

send an error message to one of the slave synchronization circuit when the difference between the actual master timestamp value and the future master timestamp value is not within a predetermined range that causes the slave synchronization circuit to take over operations as the master synchronization circuit.

15. The system according to claim 10 wherein the slave synchronization circuits adjust a received future master timestamp value according to an amount of delay associated with receiving the synchronization pulses.

16. A method for synchronizing circuitry, comprising:

identifying a period between synchronization pulses;

extrapolating a time for a future synchronization pulse by adding one of the synchronization pulses to the period multiplied by a predetermined amount.

extrapolating a master timestamp value by adding a master timestamp value for the one of the synchronization pulses and the predetermined amount multiplied by a difference between two previous master timestamp values.

receiving the extrapolated master timestamp value for an upcoming time reference in an Internet Protocol (IP) packet over an asynchronous Internet connection;

generating a local timestamp value;

comparing the local timestamp value at the upcoming time reference with the extrapolated master timestamp value;

synchronizing the local timestamp value with the extrapolated master timestamp value according to the comparison; and

receiving the extrapolated master timestamp value from a first cable modem termination system (CMTS) and using the extrapolated master timestamp value to synchronize a timing circuit in a second CMTS.

19. A method according to claim 16 including:

synchronizing the timing circuitry in the first Cable Modem Termination System (CMTS) with the timing circuitry in the second CMTS;

using the first CMTS to send data to cable modems; and

using the second CMTS to receive data from the same cable modems.

20. A method according to claim 16 further including:

receiving an error message indicating that the extrapolated master timestamp value is not equal to an actual master timestamp value for a next synchronization pulse;

predicting a new master timestamp value in response to the error message; and

sending the predicted new master timestamp value to a generation source of a message including the received extrapolated master timestamp value.

b) Claims 7, 8, 12, 13, 17, 18 are canceled:

7. (Canceled).

8. (Canceled).

13. (Canceled).

14. (Canceled).

17. (Canceled).

18. (Canceled).

4. The following is an examiner's statement of reasons for allowance:

Claims 1-6, 9-12, 15-16, 19-22 are allowed over prior art. Claims 7-8, 13-14, 17-18 are canceled.

The prior art fails to teach and render obvious the limitations as amended in the independent claims 1,10,16, and the dependent claims 2-6,9,11-12,15,19-22.

Claim 1:

“one or more line cards in the same Cable Modem Termination System (CMTS) chassis that each have local timestamp counters that is adjusted according to the received predicted master timestamp value and local timestamp value at the future received synchronization pulse and wherein the processing circuit identifies an error condition according to a number of times the local timestamp counter is synchronized with the received predicted master timestamp value.”

Claim 10;

“a processing circuit to determine, for a given count of consecutive ones of synchronization pulses cycling less often than the clocking signal”

“the processing circuit to identify the local timestamp value and synchronize the local timestamp value upon receipt of the future one of the externally generated synchronization pulses; and

one or more line cards in a same Cable Modem Termination System (CMTS) chassis that each have local timestamp counters that are adjusted according to the received predicted master timestamp value and local timestamp values at the future received synchronization pulse.”

Claim 16:

"identifying a period between synchronization pulses;
extrapolating a time for a future synchronization pulse by adding one of the
synchronization pulses to the period multiplied by a predetermined amount;
extrapolating the master timestamp value by adding a master timestamp
value for the one of the synchronization pulses and the predetermined amount
multiplied by a difference between two previous master timestamp values and
receiving the extrapolated master timestamp value from a first cable
modem termination system (CMTS) and using the extrapolated master
timestamp value to synchronize a timing circuit in a second CMTS."

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Venkatesh Haliyur whose telephone number is 571-272-8616. The examiner can normally be reached on Monday thru Friday 8:30AM to 4:30PM.

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7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application Or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Venkatesh Haliyur

Patent Examiner

EH 2/14/08

EDAN . ORGAD
SUPERVISORY PATENT EXAMINER

Edan Orgad